

in the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1 1. (Currently Amended) A computer system with improved tolerance to  
2 microprocessor functional interrupts induced by environmental sources,  
3 comprising: a microprocessor not required to be radiation hardened; an array of  
4 memory, volatile or non-volatile, connected to said microprocessor; a hardened  
5 core circuit, designed to withstand environmentally induced faults, and connected  
6 to said microprocessor, in a manner allowing for said microprocessor's interrupt  
7 control, reset control, data bus, and address bus signals to connect to said  
8 hardened core circuit, and for said hardened core's status, interrupt output and  
9 power cycle output signals to connect to said microprocessor; a microprocessor  
10 software routine configured to send a predetermined timer signal from the  
11 microprocessor to the said hardened core circuit on a predetermined time period;  
12 a hardened core circuit function configured to read the predetermined timer  
13 signal from said microprocessor on the predetermined time period and activate  
14 said microprocessor's interrupt and reset control input signals if timer signal is not  
15 received within the predetermined time period to provide for removal of said  
16 microprocessor from functionally interrupted state; a microprocessor software  
17 routine located at said microprocessor's interrupt or reset vector addresses,  
18 configured to restart the microprocessor's application software.

1 2. (Currently Amended) A system of claim 1 further comprising a microprocessor  
2 software routine configured to send maintenance data to the microprocessor  
3 memory prior to functional interrupt and configured to read said maintenance  
4 data from the microprocessor memory after microprocessor's removal from  
5 functionally interrupted state and use maintenance data to restart  
6 microprocessor's application software routines.

1 3. (Currently Amended) The system of claim 2 further comprising a  
2 microprocessor software routine configured to read said hardened core status  
3 signal(s), and to determine if interrupt or reset activation was a result of hardened  
4 core activation and then restart application software routines, or normal interrupt  
5 or reset and then continue with normal application software operation.

1 4. (Currently Amended) The system of claim 3 further comprising a  
2 microprocessor software routine configured to [to] halt all currently operating  
3 application software threads.

1 5. (Currently Amended) The system of claim 4 further comprising a  
2 microprocessor software routine configured to read hardened core status  
3 signal(s), and to determine if multiple functional interrupts occurred within the  
4 predetermined time period and then to restart all microprocessor software and  
5 hardware if multiple functional interrupts occurred within the predetermined time  
6 period, or, if single functional interrupt occurred in the predetermined time period  
7 [to] then to read maintenance data stored in said memory and provide a  
8 controlled restart of selected application software.

1 6. (Currently Amended) A computer system with improved fault tolerance from  
2 microprocessor data errors and functional interrupts, comprising: a  
3 microprocessor not required to be radiation hardened; an array of memory,  
4 volatile or non-volatile, connected to said microprocessor; a fault tolerant  
5 software routine configured to send a first instruction and at least a second  
6 instruction to the microprocessor, the first and at least the second instructions  
7 being identical and being inserted into spatially separated functional  
8 computational units of the ~~VLIW~~ microprocessor [in] at different clock cycles; a  
9 first and at least a second memory device in communication with the  
10 microprocessor, the first memory device configured to store the first instruction,  
11 the second memory device configured to store at least the second instruction; a  
12 software instruction to compare the first instruction to at least the second  
13 instruction; a comparator to compare the first instruction to the second  
14 instruction; a hardened core circuit, designed to withstand environmentally  
15 induced faults, and connected to said microprocessor, in a manner allowing for  
16 said microprocessor's interrupt control, reset control, data bus, and address bus  
17 signals to connect to said hardened core circuit, and for said hardened core's  
18 status, interrupt output and power cycle output signals to connect to said  
19 microprocessor; a microprocessor software routine configured to send a  
20 predetermined timer signal from the microprocessor to the said hardened core  
21 circuit on a predetermined time period; a hardened core circuit function  
22 configured to read the predetermined timer signal from said microprocessor [o]in  
23 the predetermined time period and activate said microprocessor's interrupt and

24 reset control input signals if the timer signal is not received within the  
25 predetermined time period to provide for removal of said microprocessor from a  
26 functionally interrupted state; and a microprocessor software routine located at  
27 said microprocessor's interrupt or reset vector addresses, configured to restart  
28 the microprocessor's application software.

1 7. (Original) The system of claim 6 further comprising a third instruction sent by  
2 the fault tolerant software routine to the microprocessor, the third instruction  
3 stored in a third memory device in communication with the microprocessor.

1 8. (Original) The system of claim 7 wherein the software instruction directs the  
2 comparator to compare the first, second, and third instruction.

1 9. (Currently Amended) The system of claim 8 wherein a match of [the]any of the  
2 first, second, and third instructions is accepted by the microprocessor.

1 10. The system of claim 6 wherein the microprocessor comprises a very long  
2 instruction word (VLIW) microprocessor.

1 11. (Currently Amended) A software and hardware computer system with  
2 improved fault tolerance from microprocessor data errors and functional  
3 interrupts, comprising: a very long instruction word (VLIW) microprocessor not  
4 required to be radiation hardened; an array of memory, volatile or non-volatile,  
5 connected to said microprocessor; a fault tolerant software routine comprising a  
6 first instruction and a second instruction, each inserted into two spatially separate  
7 functional computational units in the VLIW microprocessor at two different clock  
8 cycles and stored in a memory device in communication with the microprocessor,

9 the first and second instructions being identical; a software instruction to  
10 compare the first and second instructions in the memory device in  
11 communication with a VLIW microprocessor compare or branch units, and  
12 configured to perform an action if the first and second instructions match, the  
13 fault tolerant software routine comprising a third instruction inserted into a third  
14 spatially separate functional computational unit[s] in the VLIW microprocessor at  
15 a third different clock cycle[s] and stored in a third memory device in  
16 communication with the microprocessor, the first, second, and third instructions  
17 being identical; the software instruction to compare the first, second, and third  
18 instructions in the memory devices in communication with a VLIW  
19 microprocessor compare or branch units, and configured to perform an action if  
20 any of the first, second and third instructions match; a hardened core circuit,  
21 designed to withstand environmentally induced faults, and connected to said  
22 microprocessor, in a manner allowing for said microprocessor's interrupt control,  
23 reset control, data bus, and address bus signals to connect to said hardened  
24 core circuit, and for said hardened core's status, interrupt output and power cycle  
25 output signals to connect to said microprocessor; a microprocessor software  
26 routine configured to send a predetermined timer signal from the microprocessor  
27 to the said hardened core circuit on a predetermined time period; a hardened  
28 core circuit function configured to read the predetermined timer signal from said  
29 microprocessor [o]in the predetermined time period and activate said  
30 microprocessor's interrupt and reset control input signals if the timer signal is not  
31 received within the predetermined time period to provide for removal of said

32 microprocessor from functionally interrupted state; and a microprocessor  
33 software routine located at said microprocessor's interrupt or reset vector  
34 addresses, configured to restart the microprocessor's application software.

12. (Canceled)

13. (Canceled)